Proximity effect of electron beam lithography for single-electron transistor fabrication

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In this letter, we shall describe a method, utilizing the proximity effect in electron beam lithography, suitable for fabricating silicon dots and devices, and demonstrate the electronic characteristics of the Si single-electron transistor. The drain current ($I_D$) of the device oscillates against gate voltage. The electrical characteristics of the single-electron transistor were observed to be consistent with the expected behavior of electron transport through gated quantum dots, at up to 150 K. The dependence of the electrical characteristics on the dot size reveals that the $I_D$ oscillation follows from the Coulomb blockade by poly-Si grains in the poly-Si dot. The method of fabrication of this device is completely compatible with complementary metal–oxide–semiconductor technology, raising the possibility of manufacturing large-scale integrated nanoelectronic systems. © 2004 American Institute of Physics. [DOI: 10.1063/1.1811803]

Recent years have seen dramatic developments in nanometer-scale silicon (Si) structures and especially in silicon nano devices that utilize the quantum or single-electron charging and low power consumption features of a single-electron transistor (SET), which make them promising basic elements for microelectronic and nanoelectronic circuits in the future. The main limitation, which tends to hinder progress in this direction, is the requirement of very small structural elements in the devices. For operation at room temperature, the devices should be smaller than 10 nm, below the limit of resolution of modern nano-lithography processes.

Electron beam lithography is a technique for creating extremely fine patterns (0.1 μm and below) for integrated circuits. Such patterns can be made because the spots of electrons are very small, whereas the optical lithography is limited by the wavelength of light used for exposure. The wavelength of the electron beam is so small that diffraction no longer determines the lithographic resolution. Accordingly, electron-beam lithography is the most commonly used technique in this field, and many researchers have been investigating its application to make nanopatterns.

In electron-beam lithography, the well-known proximity effect refers to variation in the width of patterned lines with the density of other shapes nearby, which variation of course makes increasing the resolution difficult. The electron proximity effect has been a major obstacle to achieving fine resolution in electron-beam lithography. As charged particles, electrons undergo forward and backward scattering when they are incident to a resist layer on a substrate. The scattering of these electrons causes undesirable resist development energy to accumulate around the patterned areas. This accumulated energy from the scattered electrons only slightly affects isolated patterns, but significantly more energy accumulates in densely patterned areas. Hence, isolated patterns are somewhat narrower than designed, and lines in densely patterned areas are somewhat wider than designed. The distribution of intensity of exposure has a Gaussian intensity profile, because electrons are forward scattered and backscattered. The main ways to compensate for the proximity effects are to adjust the dosage of the electron beam according to the density of the patterns, or to anticipate the changes in dimensions of the features and make compensating adjustments in advance. Nevertheless, this work reports the fabrication of SETs from silicon point contact, made by exposing different shapes in the pattern to incident electrons with various intensities.

The point-contact structures are fabricated by choosing an appropriate electron-beam dose and pattern development time. The substrates used in this work were $p$-type Si substrates, with a thin 25 nm poly silicon layer on top of a 200-nm-thick buried SiO$_2$ layer. The top poly silicon layer was doped by phosphorous in a low-pressure chemical vapor deposition (LPCVD) system and annealed at 925°C for 20 min in a nitrogen atmosphere. The sheet resistance of the poly silicon layer is around 25–50 Ω/cm$^2$ at room temperature. The point-contact structures were formed by direct writing electron beam using a Leica Weprint 200 system with a NEB22A electron-beam resist and a transformer coupling plasma silicon dry etcher. The 40 keV acceleration voltage of the Leica Weprint 200 system yielded a fine beam with a diameter of about 20 nm; the beam current density was 4 A/cm$^2$. After exposure to the e beam, the pattern was developed by a hydroxide-based developer, and baked at 115°C for 120 s. Figure 1 schematically depicts the mechanism used in this work for forming point-contact structures. When the resist is exposed to the electron beam at the tip of each electrode (at distance between the tips of the electrodes of 90, 100 and 110 nm), then the resist in the interelectrode region is also partially exposed because the beam has a Gaussian intensity profile (indicated by the dotted lines (middle)). Since the designed gaps of 90, 100, and 110 nm are close to actual beam size, both beams overlap in the gap region. Therefore, an overall beam dose whose profile is described by a solid line (bottom) interacts with the resist in...
this region. Consequently, after developing, the area dosage remains higher than threshold exposure dosage and forms a point-contact structure. Finally, etching is performed in LAM TCP 9400SE, using 5–20 mTorr mixing in an atmosphere of Cl₂, O₂, HBr and SF₆ at 65°C. Figure 2 shows the scanning electron micrograph of the 20 nm x 20 nm point-contact structure. After the pattern had been transferred, a 5-nm-thick gate oxide was grown at 925°C for 2.5 min in oxygen, further reducing the point-contact dimension. Then, 50-nm-thick n-type poly-Si was deposited by a LPCVD system to form the control gate. The gate poly-Si was lithographically patterned and etched to cover the Si point-contact structure. After another 200-nm-thick tetra-ethyl-ortho-silicate oxide layer was deposited and contact patterning performed, an aluminum metal film was deposited and patterned to provide electrical contacts to the device. A HP4156 B semiconductor parameter analyzer measured the characteristics of the device at 300 K in air and at low temperatures from 4 up to 150 K in a liquid He-4 system, with Keithley 4200 semiconductor characterization system.

The point-contact device was characterized electrically from 4 to 300 K. The source-drain current (Iₚ) was measured with respect to the source-drain voltage (Vₚ) and the gate voltage (Vₙ), and single-electron effects were observed over the entire temperature range. Figure 3 plots single-electron current oscillations in the Iₚ–Vₙ characteristics at 40 K. Vₚ increases from −10 to 10 mV in 1 mV steps. Oscillations with multiple periods are observed; these may be associated with single-electron charging in a multiple dominant charging island. The increase in the background current with gate voltage, similar to that of SETs fabricated in crystalline silicon, may be explained by a metal–oxide–semiconductor field effect transistor-like field effect. At lower temperature of 4 K, the characteristics are more complicated and additional oscillations in Iₚ are observed. These effects may be associated with single-electron charging in multiple grains in the point contact. These peaks manifest the fact that the electrostatic energy, when the bulk electrode contains N excess current carriers, equals that when the quantum dots contain N + 1 excess carriers. Therefore, the current carrier passes the quantum dots to the other bulk electrode by tunneling through the barriers on each side of the quantum dots. When the energy equality does not hold as the electric potential of the gate electrode, the quantum dots are in a stable condition for containing an integer number of current carriers, and no current can flow through the device, which is known as a Coulomb blockade region according to orthodox theory. Figure 4 plots the dependence on temperature of current oscillations on temperature; these oscillations persist up to 150 K with a period ΔVₚ ≈ 0.5 V. The fine structure superimposed on the oscillations disappears at 150 K, corresponding to a gate-island capacitance Cₕ = e/ΔVₚ = 3.2 aF. The current oscillations are superimposed on a generally increasing current background, resulting in a nonzero valley current in the oscillations. This behavior has also been observed in nanowire multiple-tunnel junction single-electron transistors, fabricated in silicon-on-insulator material, and may be related to a field-induced enhancement of the carrier concentration in the device. The gate may also increase in the tunneling probability. Figure 5 plots Iₚ as a function of Vₙ and Vₚ: the curves are the constant Iₚ contours. The straight lines emphasize the
rhombus-like region of the plot. In the rhombus, the nano-dots stably contain an integer number of electrons. Thus, the current that flows through the quantum dots is drastically reduced due to Coulomb blockade effect under the conditions defined by \( V_g \) and \( V_d \) in the rhombus-like region. These observations are consistent with the predictions of the orthodox theory of the operation of SET. Furthermore, the slopes of the straight lines that define the rhombus-like region provide important information about the nano-dots. The experimental values of the control gate capacitance \( C_g \), the drain capacitance \( C_d \), the source capacitance \( C_s \), and the total capacitance \( C_S \) can be experimentally determined. The two slopes of the edges of the rhombus-like region are 3.3 and 2.67, which equal \( C_d/C_g \) and \( (C_d+C_s)/C_g \), respectively. The range \( (|V_d|) \) of the drain-source voltage \( V_d \) from 0 mV to the tip of the rhombus-like region is \( 10–15 \) mV. Accordingly, the total capacitance \( C_S=C_g+C_d+C_s \) calculated from the range of \( V_d \) according to \( C_S=e/|V_d| \) is \( 10–16 \) aF. Solving for \( C_g, C_d, \) and \( C_s \) yields \( C_g=1.78–3.2 \) aF, \( C_d=2.97–2.24 \) aF, and \( C_s=5.87–10.56 \) aF. The threshold voltage \( V_T \) is obtained as \( 10–15 \) mV from the Coulomb diamond graph. Then, the \( C_S \) is derived at about \( 10–16 \) aF, considering that \( \sim 42\% \) of 450 devices that were measured yielded total capacitance \( C_S \) around \( 10–16 \) aF for each device. The theoretical value of the control gate capacitance \( C_g \) can also be approximated. The width of the nano-dots defined is 20 nm. Additionally, the thickness \( D \) of the gate oxide, which equals the distance between the control gate and the dots, is 5 nm. Therefore, \( C_g \) is estimated as \( C_g=e_e e_a A/D \), where the relative dielectric constant \( e_r \) of silicon dioxide is 3.9, so \( C_g \) is 3.5 aF, which value is consistent with the previous calculated value 1.78–3.2 aF. The Coulomb dots should therefore be smaller than 15 nm (width) \( \times \) 15 nm (length) \( \times \) 20 nm (thickness).

In conclusion, silicon point-contact devices were fabricated on a poly silicon film. The devices were fabricated based on the proximity effect associated with electron beam lithography, alleviated by exposing various shapes in the pattern to electrons with various intensities. The devices consist of top-gated quantum dots between the source and drain electrodes. The electric characteristics of the devices included single-electron charging effects up to 150 K. The fabrication of the device is compatible with silicon technology, raising the possibility of manufacturing large-scale integrated nanoelectronic systems.

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