An Automatic Analog Layout Design System

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ABSTRACT

A prototype system for efficient layout of analog circuits has been developed. A slot partition based method is used to parse the functionality of analog circuits. Detailed implementation of the automatic design system is described. Experimental results demonstrate that the proposed prototype system can effectively produce high-quality artworks to meet the matching, symmetry, etc. constraints of typical analog circuits.

(KEY WORDS: layout, analog circuits, automatic design system.)
I. INTRODUCTION

The rapid advances in IC fabrication technology cause VLSI chip complexity to increase. The technologies of the new generation allow to design mixed analog/digital circuits and systems. To meet the challenge of ever-increasing design complexity, it is inevitable to use computer-aided design tools to reduce the costs of the sophisticated IC design process. The automation of the digital design can be managed efficiently using CAD tools developed for semicustom design methods such as gate arrays, standard cells, and macro cells. Although these automated layout technique have advantages in the digital domain, they are not suitable for the analog circuits.

There are various reasons why design automation for analog circuits is different from its digital counterpart. The principal reason is largely due to the many interacting layout constrains which affect the functionality of the circuit. Typical of these layout constraints include matching, symmetry, limited parasitic and signal coupling. Furthermore, the large variation in L/W ratios causes the analog circuit components with irregular shapes and dimensions. This irregularity makes the layout process even more difficult.

Substantial research effort is being devoted to developing analog cell generator systems. ILAC[7] has a number of attractive features, however, the use of the system is limited because only algorithmic principles are employed. The layout generated by ILAC are on the average 25 percent larger than a hand-crafted layout. In ACACIA/ANAGRAM[2], a cost function in terms of routing parasitics is used, it lacks a global view of the interaction of device placement and detailed routing. OPASYN[4] uses accumulated design experience to partition an analog circuit into a slicing tree. Even the use of shape function achieving better matching on cell aspect ratio, the limitations of the design experiences on special circuits make it difficult for the cell generator to be applied to a general circuit.

This paper presents a prototype system called LAKE(Layout Analog Kit Expert), developed for efficient layout of analog circuits. LAKE is to be able to derive mask level information from a given structural specification. The approach adopted in LAKE is in many respects quite different from the techniques described above. In stead of considering routing and placement as two independent problems, LAKE treat place-and-route as a single procedure[6]: The most novel feature of LAKE is its unique ability to recognize performance related layout structures directly from circuit schematics. Section 2 describes an overview of the LAKE system. Section 3 describes the implementation of the system and presents the heuristic place-and-route procedure which plays a key part in the way that the system achieves its results. Section 4 contains experimental results and an example to illustrate the operation of the system. Conclusions are presented in section 5.

II. SYSTEM OVERVIEW

A block diagram of the analog IC layout system is given in Figure 1. The netlist information is treated as the input database to the system. The methodology adopted in the
LAKE system is integrated to produce the final geometry layout. This system typically involves four primary tasks:

1) a netlist translation process,
2) a network partitioning and ordering process,
3) a slot generation process,
4) a performance driven place-and-route process.

![System block diagram.](image)

The procedure begins by parsing an input netlist file describing the circuit structure and the desired performance. The circuit parameters include the device size, device type, and device netlist are stored in a C-like intermediate description file. The entire network is viewed as a directed graph and then is partitioned into several slots. The partitioning strategy is basically to group sensitive devices such as matched transistors or strongly connected devices which have common-channel-path between source and drain nodes. Based on the partition analysis, a slot with various device geometry layouts are generated to minimize diffusion line length and avoid undesirable coupling between critical signal nets. The cost function of a slot is computed to facilitate the place-and-route process. The simulated-evolution placement technique[5] is applied to slot placement. In the routing stage, the sensitive nets within the slot will be routed first. Finally, channel routing performs detailed local routing within each channel. This iterative place-and-route procedure will be performed to complete wire interconnection with minimal wire parasitic.
III. PHYSICAL IMPLEMENTATION STRATEGY

LAKE system shown in Figure 1 with an integrated set of interacting tools has been implemented in C language. These tools are all interfaced with the Cadence Edge Framework. the LAKE system consists of an internal data base which contains the netlist descriptions, slot descriptions, the digraphs for network partitioning.

3.1 Input Netlist

The input netlist of the sized circuit schematic is parsed by an input netlister which is a translation processor to produce a C-like intermediate input description file. The netlister extracts the netlist information from the schematic circuit. Meanwhile, the properties of each components in the schematic circuit are parsed by the netlister. The data structure used in the netlister is given here:

<table>
<thead>
<tr>
<th>variable type</th>
<th>function description</th>
</tr>
</thead>
<tbody>
<tr>
<td>char szName[16];</td>
<td>/* Component name. */</td>
</tr>
<tr>
<td>char szMName[16];</td>
<td>/* Model name. */</td>
</tr>
<tr>
<td>int iMType;</td>
<td>/* Model type: nMOS, pMOS... */</td>
</tr>
<tr>
<td>int iNode[4];</td>
<td>/* Node properties. */</td>
</tr>
<tr>
<td>char szParas[128];</td>
<td>/* Device property parameter. */</td>
</tr>
</tbody>
</table>

3.2 Network Partitioning and Ordering Process

For an analog IC network \( \Omega(N,D) \) consists of a set of nodes N interconnected by a set of devices D, the network descriptions can then be extracted directly from the intermediate input description file. A rooted-digraph \( G(V,E) \) is further constructed based on \( \Omega(N,D) \).

Each vertex \( V \) in \( G \) represents several geometrical and process parameters, such as the type of device, the transconductance parameter, etc. Each edge \( E \) has its associated function \( f \) which tells how the signals pass from one end to the other. If \( P \) is a path consisting of devices \( D_1, \ldots, D_n \) with associated functions \( f_1, \ldots, f_n \) then the function associated with the path \( P \) is \( f_n f_{n-1} \ldots f_1 \), which we denote by \( f_p \). If the edge connected two transistors which abutted together from source of one transistor to drain of another transistor, then its associated function is \( f_{\text{strong}} \). If an edge terminated at the gate of a transistor or passive components, then its associated function is \( f_{\text{weak}} \).

We will use the symbol \( \Sigma \) to denote the set of partitioned-slot in the network, and henceforth, we shall refer to the partitioned network as \( \Omega(N,D,\Sigma) \). If \( f_i \) is a set of vertices in a strongly-connected component of \( G \), then the corresponding set \( \Sigma_i \) will form a strong-connected slot. Similarly, a weak-connected slot can be defined. Thus, we have a partition \( \Sigma_1, \Sigma_2, \ldots, \Sigma_n \) of the slots in \( \Omega(N,D,\Sigma) \). The \( f_p \) is found by the depth first search algorithm and a branch-and-bound procedure[8] is performed. \( f_p \) can be analyzed to be matched.
groups, symmetry groups which can avoid undesirable cross coupling constraints and presserve symmetric placement and routing.

3.3 Slot Generator

The network partition $\Sigma$ obtained from the previous synthesis phase together with the digraph information, and a reference to a technology file provide necessary information for the slot generator. The slot height is then calculated to be the square root of the whole cell area. The whole cell area is estimated as the sum of the area of each device component plus an additional 20 percent area for routing. Therefore, the cell aspect ratio can be adjusted using the following equation:

$$Cell_{\_\_\_\_height} \equiv \sqrt{Cell_{\_\_\_\_Area}} \div n \equiv Slot_{\_\_\_\_height}$$

(1)

where $n$ is the cell aspect ratio.

In addition, it is common for an analog MOS transistor with large W/L ratio. In order to reduce the parasitic capacitances and W/L ratio, a stacked structure is automated generated to meet the specifically geometrical constraints. The slot description database is applied to adjust the shape and area of the various devices to fit into the predefined slot.

3.4 Performance Driven Place and Route

We implemented the cost function of slot placement as a weighted average of the diffusion line length and the number of wire crossings. The routing path for each net is determined by $f_r$. The cost function of routing is estimated as manhattan distances. Channels with fully symmetric nets are routed first. The channel router based on the left edge algorithm is implemented[3]. The above routing strategy reduces the crosstalk noise; however, it cannot always find the optimum routing path. The place-and-route procedure will be further improved by iterative simulated evolution method. Figure 2 shows the three major steps that are evaluation, selection, and allocation in the iterative loop of the simulated evolution procedure.
VI. EXPERIMENTAL RESULTS AND DISCUSSION

This section presents an example to show the mask level layout generated by the LAKE system from its schematic topology. Figure 3 is an operational amplifier circuit with the detailed W/L ratios of the transistors. The artwork is generated within the Cadence OPUS system. The 08DPDM technology file[1] provided by Chip Implementation Center, National Science Council is used in our present work.

Mask level layouts with specified aspect ratios of 1 and 2 are shown in Figure 4 and Figure 5, respectively. For this example, the CPU time on a Sun Sparc is less than 3 seconds. A summary of some quantitative data is given in Table 1. The device density is the cell area divide by the sum of the area of all the components in the circuit schematic. From Table 1, it is shown that the routing area is about 20% of the total cell area for the present example. It also demonstrates that our system can be flexible of adjusting the aspect ratios based on the user's defined values. In addition, the results are in good agreement with Eq(1).

Figure 2. The main loop of simulated evolution process applied for place and route procedure.

Figure 3. The experimental schematic circuit and its corresponding digraph obtained from netlister analysis.
Figure 4. The mask level layout with specified aspect ratio 1.

Figure 5. The mask level layout with specified aspect ratio 2.

Table 1. The cell area, aspect ratio, and device density of the illustrated example.

<table>
<thead>
<tr>
<th></th>
<th>Cell Area ($\mu m^2$)</th>
<th>Aspect ratio ($\mu m / \mu m$)</th>
<th>Device density</th>
</tr>
</thead>
<tbody>
<tr>
<td>Figure 4.</td>
<td>13,200</td>
<td>1.32(132/100)</td>
<td>1.18</td>
</tr>
<tr>
<td>Figure 5.</td>
<td>13,770</td>
<td>1.91(162/85)</td>
<td>1.23</td>
</tr>
</tbody>
</table>
V. CONCLUSIONS

A prototype system that automatically produce geometrical layout for analog circuits is demonstrated. The proposed prototype system was implemented in C on a Sun Sparc workstation. The integrated set of interacting tools include behavioral, structural partition synthesis. Furthermore, the Cadence Edge Framework can be used interactively to modify the design if needed, and the final layout can be simulated with extracted parasitic capacitances. Future work is centered on finalizing the implementation of maximum regularity extraction to further simplify the complexities of the analog layout problems.

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