Pre-Intrinsic Gettering Treatment Of CZ Silicon Substrate For The Yield Of Semiconductor Device

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ABSTRACT

This paper presents results of the effect of pre-intrinsic gettering treatment of cz silicon substrate. Material parameters, including the preintrinsic thermal cycle, will be Presented. Minority carrier lifetime and leakage current correlated to dram refresh time and mwmory yield improvement will be discussed.

(KEY WORDS : intrinsic gettering ; yield ; denuded zone)
I. INTRODUCTION

Telecommunication feature-rich products require processes to deliver circuits consisting of a variety of medium-size circuitry on the same die. In general a typical circuit may include analog circuits, timing clock, digital logic, I/O logic as well as various quantities of SRAM, ROM and DRAM. For such circuitry, fabrication process parameters are chosen to maximize overall chip performance rather than to optimize the performance of any individual circuit. Also, due to the different environments they are required to operate over a very wide temperature range between -65 °C to 100 °C. At this high temperature, small leakage currents, generated in or near an active region, may cause memory refresh problems.

The complexity of integrating all such device structures simultaneously has forced the fabrication processing to utilize low temperature process steps to reduce the dependence of one step on another. Therefore it makes difficult to full utilization of external gettering techniques where the action is confined to a particular process temperature. Under such circumstance, pre-intrinsic gettering treatment before actual device processing is necessary to improve device performance and yield. However this technique required a rather long period temperature annealing, it would not be able to accept by I.C. manufacture. In order to overcome this weak point, and enhance the nucleation and precipitation of oxygen, pre-intrinsic gettering with slow ramping rate was used [6]. For the intrinsic gettering, initial oxygen content affects denuded zone depth (DZD), and bulk microdefect (BMD) formation, which in turn influence both refresh time of DRAM and circuit yield. Uncontrolled oxygen concentration can result in adverse effects. Optimization of the oxygen content of wafers for DRAM process is a complex interplay of various material parameters and electrical parameters. Too much precipitation may cause core slip, warpage and insufficient denuded zone depth [3,4]. Defects in active device regions enhance leakage of PN junctions and MOS capacitors. Too little precipitation may result in thermal donor problem and insufficient gettering ability [2]. For a given device process, there is an optimum \( \Delta[O] \) which produces the right combination of BMD and DZD for maximum device yield. It was suggested that the critical initial oxygen concentration of approximately 15 to 20 ppm, precipitation of approximate \( 10^6 \text{cm}^{-2} \) microdefect density and 10-40 \( \mu \text{m} \) thick denuded zone would be enough for intrinsic gettering purpose. [1]. The goal of this work was to evaluate the effect of denuded zone formation and intrinsic gettering on DRAM refresh time. Also the pre-intrinsic gettering thermal cycle and the process flow will be described. The resulting substrate will be analyzed. Substrate minority carrier lifetime and diode leakage current will be presented and correlated to memory refresh time. Yield improvement for DRAM operation will be discussed.

II. FABRICATION

Silicon starting substrates used were 150mm, (100)CZ Si, Boron-doped, 15\pm2 ohm-cm resistivity, oxygen content 15\pm2 ppm, and carbon content <1 ppm. Some of the starting material was given a thermal treatment with a slow ramping rate of 2 °C/min as shown in Figure 1. This three-step pre-thermal cycle was used to obtain a denuded zone layer approximately 40 \( \mu \text{m} \) thick followed by nucleation and growth of bulk microdefect density
around $10^4 \text{cm}^{-2}$. Figure 2. shows a cross-sectional micrograph of the defect-free zone and the bulk micro-defect region after preferential etching. The creation of a wide denuded zone reduces the material surface defect density. Then wafers which with and without pre-annealing were processed through. The process, which was a typical MOS process was shown in Figure 3. The main thermal cycle of the process temperatures used include 950 °C for LOCOS field oxide, 1000 °C N-well drive, and 950 °C for gate and capacitor oxide formation. At these temperatures the effective diffusion length of impurities or metallic contaminants will be sufficient to reach the bulk defect region, and be effectively gettered there.

III. MEASUREMENTS

Typical test device structures were shown in Figure 4. The parameters measured at room temperature, for P and N transistor were normal minority carrier lifetime of constant capacitance c-t measurements and junction leakage current measurements, on substrates with and without intrinsic gettering, were summarized in Table I. If the refresh time of one-transistor memory cell was less than 10ms, the die was considered defective. [5] Table II shows the relative yield and refresh time loss for intrinsically gettered and non-gettered wafers. It is shown that yield and the refresh time are greatly improved.

IV. SUMMARY

The effect of denuded zone formation and intrinsic gettering in silicon starting substrates on MOS process was studied. A three-step with slow ramping rate thermal cycle was used. It generated a 40μm wide denuded zone and bulk microdefect density of $10^6$ per $\text{cm}^2$. The substrate minority carrier lifetime improve by 20% and junction leakage current was reduced by 3 times. The device yield and refresh time loss were improved by 77% and 30% respectively for intrinsically gettered wafers.

V. ACKNOWLEDGMENT

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VI. REFERENCES

of 2nd Symposium on Defect in Si ECS p.589 Sept. 1991


Fig.1 Pre-initial three-step intrinsic gettering cycle

Fig.2 Cross section of gettered substrate
Main thermal cycles of MOS integrated circuit process flow

- Pre-intrinsic thermal cycle
- First pad oxidation 950°C O2 45min 300 Å
- Alignment wet oxidation 950°C 4hrs 6000 Å
- N-well Drive 1000°C 8hrs
- Second pad oxidation 950°C 45min 300 Å
- LOCOS Field 950°C 5hrs oxidation
- 1st and second gate dry oxidation 950°C 2*15min
- Backend low temperature process

Fig. 3

Table 1. Minority carrier lifetime and junction leakage current

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<thead>
<tr>
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<th>Intrinsic gettering</th>
<th>Without intrinsic gettering</th>
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<tr>
<td>Average minority carrier lifetime</td>
<td>44.8</td>
<td>36.23</td>
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<tr>
<td>(μs )</td>
<td></td>
<td></td>
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<tr>
<td>Average junction leakage current</td>
<td>2.6</td>
<td>9.16</td>
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<td>(PA)</td>
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Table 2. Relative yield and refresh time loss

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<thead>
<tr>
<th></th>
<th>Without gettering</th>
<th>Gettering</th>
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<tbody>
<tr>
<td>Good die %</td>
<td>23</td>
<td>100</td>
</tr>
<tr>
<td>Refresh time loss %</td>
<td>100</td>
<td>71</td>
</tr>
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Fig. 4 Test device structures used for Measurement of capacitance as a function of time (a). The measurement of the (leakage) currents as a function of (reverse) voltage $V_s$ (b). one-transistor DRAM cell (c)